Before starting, permissions to use Synopsis tools is needed through the lab. And the first time you need to copy this folder

cp -r /users/iit/synopsys/tsl018\_20178\_syn design\_syn

1. Start in the src/ips/riscv folder
2. Move all contents if the include folder to the riscv folder
3. Type the following commands
   1. > cd design\_syn
   2. > dc\_shell
   3. >Start\_gui
   4. In the gui: File-> analyze ->add include/\*

If it gives you errors, it’s probably because of the files themselves including each other. So try adding them one by one in the following order (worked for me):

riscv\_defines

riscv\_config

apu\_macros

apu\_core\_package

* 1. Don’t add the tracer files.

1. In the gui: File->analyse->add riscv/\*(but uncheck the include files ,the riscv\_tracer files, test(I added it just for testing) and riscv\_register\_file\_latch)

It gave me the error that in riscv\_register\_file.sv:27 the module riscv\_register\_file is redefined (VER-25). In the dc-shell, I ran `man ‘VER-25’ ` and found that this error indicates that there are two modules with the same name which synthesis does not allow. Found the problem was that I included the riscv\_register\_file\_latch which includes the declaration of module ‘riscv\_register\_file’ like is included in the riscv\_register\_file.sv file. These two files are mutually exclusive and should never be together in the same synthesis. The riscv\_register\_file is for ASIC synthesis, and the riscv\_register\_file\_latch is for FPGA synthesis (according to the spec).

1. File - > Elaborate
2. Choose the library to be WORK and the top-level module to be riscv\_core
   1. We got an error : width mismatch in riscv\_custom.sv- enable\_i
      1. This was fixed by changing to the instantiation of the module riscv\_custom inside of riscv\_ex\_statge and changed the .enable\_i( ‘b0) to .enable\_i(1’b0)
3. Design -> Comile Design
4. After compilation: file->save as <name>
5. Click open
6. file -> read <name>
7. In the logical hierarchy pane right click on the top-level module and select schematic view. Then you’ll be able to watch the synthesized file in gate level (if you wish). Notice that if you do the schematic view on the rtl files (elaboration) you’ll be able to see logic gates but the names on them would start with gtech which means ‘general technology’. After synthesis, however, the names would be the technology names.
8. You may now make timing reports
   1. How to read:
   2. You have point which is the name of the netlist reference. Then you have 2 columns: the Incr and the Path. The whole list gives you one critical path, the Incr is by how much time does the specific cell increment the critical time path, and the Path tells you the sum of the Incr along the critical path.